

Notice of References Cited	Application/Control No. 09/922,639		Applicant(s)/Patent Under Reexamination PARVATHALA ET AL.	
	Examiner CHAMELI C DAS		Art Unit 2122	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,572,712	11-1996	Jamal, Kamran	716/18
	B	US-6,400,173	06-2002	Shimizu et al.	324/765
	C	US-6,708,305	03-2004	Farnsworth et al.	714/739
	D	US-6,553,527	04-2003	Shephard, III, Philip George	714/733
	E	US-6,769,081	07-2004	Parulkar, Ishwardutt	714/733
	F	US-6,658,611	12-2003	Jun, Hong-Shin	714/719
	G	US-6,415,403	07-2002	Huang et al.	714/726
	H	US-6,769,115	07-2004	Oldman, Daniel E.	717/126
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	TITLE: BIFEST: A Built-in Intermediate Fault effect sensing and test generation system for CMOS Bridging faults, author: Lee et al, ACM, April, 1999.
	V	TITLE: Built-in Self-Test with an alternating Output, author: Bogue et al, IEEE, 1998.
	W	TITLE: Built-In Test Sequence Generation for Synchronous Sequential Circuits Based on Loading and Expansion of Test Subsequences, author: Pomeranz et al, ACM, 1999.
	X	TITLE: Concurrent Test Scheduling in Built-In Self-Test environment, author: Chen et al, IEEE, 1992.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.